Docket No.: P2001,0216

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	:	10/673,705	Confirmation No.:	2451
Inventor	:	Annalisa Cappellani et al.		
Filed	:	September 26, 2003		
TC/A.U.	:	2829		
Examiner	:	Scott B. Geyer		

DECLARATION TO ACCOMPANY PETITION UNDER 37 C.F.R. 1.8(b) and 1.10(c)

I, Laurence A. Greenberg, hereby declare that:

- to the best of my knowledge and belief, the mailing of September 26, 2003 was sent by Express Mail to the Patent and Trademark Office on that date;
- to the best of my knowledge and belief, the mailing of October 23, 2003, was sent by first class mail to the Patent and Trademark Office on that date;
- I have reviewed the pertinent pages of the outgoing mail log for September 26, 2003, and October 23, 2003, and the pages show that the papers as listed in the accompanying amendment were indeed mailed on the dates indicated above;
- the mailing of October 23, 2003 was originally signed by Mark Weichselbaum who is no longer with the firm.

LAURENCE A. GREENBERG
REG. NO. 29,308

Laurence A. Greenberg

Date:

LERNER AND GREENBERG, P.A.

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Denise A. Lettau (DC Bar)
Yonghong Chen (Chinese Pat. Agent)
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Kyle H. Flindt (UT Bar)

Of Counsel:
Herbert L. Lerner (NY Bar)

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner for Patents, Alexandria, VA 22313-1450.

MICHAEL BURNS

Docket No.: P2001,0216

Date: September 26, 2003

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : ANNALISA CAPPELLANI ET AL.

Title : METHOD FOR FABRICATING A MOSFET HAVING A VERY SMALL CHANNEL LENGTH

1 sheet of drawings.
The payment in the amount of $750.00 covering the filing fee.
PCT Cover Sheet WO 02/078058 A2
Information Disclosure Statement and 15 References.

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(f). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Applicants
LAG:kf

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P2001,0216; P2002,0797; P2001,0226; F-8351

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DOCKET NO. P2001.0216 ..... Mailed September 26, 2003

APPLIC. NO. ..... Express Mail EV309760700US

The stamp of the Patent Office hereon may be considered the date on which papers indicated below were received.

Applic pgs 20 Rule 53b New ☒ Contin ☐ Div ☐ CIP ☐ / Rule 53c Prov. ☐ / Rule 53d CPA ... RCE ☐

☐ CIP ... pgs ☐ Design ☒ 1 Dwgs ☐ Declaration ☒ Mailing Certif.

☐ Priority Claim ☐ Cert. Prior. Doc(s) ☒ PCT Cover Sheet WO 02/018058 A2

☐ Amend pgs ... ☐ Prel. Amend pgs ... ☐ Letter

☐ Response pgs ... ☐ 37CFR1.116 ☐ Not. of Appeal

☐ Brief pgs ... ☐ Appndx pgs ... ☒ I.D.S. + 15 Refs.

☐ Assoc Pwr of Atty ☒ Credit Card $ 750.00

☐ Pet. for Ext .... Mo. ☐ Pet .... ☐ Check $ ....

☐ Issue Fee ☐ Assignment ☒ PTOL 1449.

☐ Cert. Trans. ☐ Cert. of Corr. ☐ File rec. corr

Intern Search Report .....

22386 U.S. PTO
10/673705

U.S. POSTAGE

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P.O. Box 2480
Hollywood, FL 33022-2480

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Docket No.: P2001,0216

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : ANNALISA CAPPELLANI ET AL.

Filed : CONCURRENTLY HEREWITH

Title : METHOD FOR FABRICATING A MOSFET HAVING A VERY SMALL CHANNEL LENGTH

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 6,091,120 (Yeom et al.), dated July 18, 2000;

U.S. Patent No. 5,089,863 (Satoh et al.), dated February 18, 1992;

U.S. Patent No. 5,384,479 (Taniguchi), dated January 24, 1995, and corresponding German Patent DE 42 34 528 C2 (Taniguchi), dated April, 15, 1993;

German Published Non-Prosecuted Patent Application DE 42 34 777 A1 (König et al.), dated April 21, 1994, and English abstract thereof;

French Patent Application FR 2 791 177 A1 (Thomas et al.), dated September 22, 2000, and English abstract thereof;

Patent Abstracts of Japan 63044768 (Shinichi), dated February 25, 1988;

European Patent Application EP 0 740 334 A2 (Eckstein et al.), dated October 30, 1996;

European Patent Application EP 0 328 350 A2 (Nakamura et al.), dated August 16, 1989;

PCT WO 02/41383 A1 (Furukawa et al.), dated May 23, 2002;

Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2nd Edition, pp. 201-203;

Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418;

Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of $TiSi_2$ and $CoSi_2$ ", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269;

Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1-μm CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956;

Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs", IEEE, 1994, pp. 497-500;

International Search Report, dated April 14, 2003.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Applicants

Date: September 26, 2003

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/nt/kf

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Mail Docket
2003

DOCKET NO.	INVENTOR	Amend (No. of Pgs.)	Amend 1.116 (No. of Pgs.)	Appeal	Application (No. of Pgs.)	Assignment	Brief	Cert. Correction	CIP	Claim for Priority	Declaration	Divisonal	Express	Fil. Rcpt. Correct.	Formal Drawings (No.)	IDS (No. of Refs.)	Inf. Drawings (No.)	Issue Fees	Letter	Letter Draftsman	Maintenance Fee	PCT Cover Sheet	Petition for Ext.	(Ass.) Power of Attorney	Priority Document	RCE	Response	Trademark Application	1533	$ Amount	$ Amount	Credit Card	Check	Addit. Info.
26-Sep-03																																	
A-3902	Lorenzi				10						X		X		4	13						X							$1,080.00		X		PCT, 02/078916A2+A3, Fee Calc
P2002,0797	Scherer				14					X			X		2	8									X				$750.00		X		1449
P2001,0226	Muschallik				47					X			X		18	10						X			X				$750.00		X		1449, ISR, 02/078200A2
P2001,0216	Cappellani				20								X		1	15						X							$750.00		X		1449, ISR, 02/078058 A2
F-8351	Levine				36						X		X		15	6													$505.00		X		1449, Pet. To accept col. Photos
F-8351 PCT	Levine												X		15														$2,170.00		X		PCT, Fee Calc. Sheet, Transm. L
A-3231	Bitterich																	X											$1,600.00		X		85B, Pub. Fee
SBV-08685	Lippert					X												X											$1,600.00	$40.00	X		85B, Pub. Fee, 1595
GR98P8644	Alsmeyer					2												X											$1,600.00	$80.00	X		85B, Pub. Fee, 1595
2000P1278	Wörz					X												X											$1,600.00	$40.00	X		85B, Pub. Fee, 1595
E-41047	Brück					X												X											$1,300.00	$40.00	X		85B, 1595
P2002,0587	Hanuschek									X															X								
M&N-IT-471	Weigel															8																	1449
P2002,0578	Willer																							X		1							
P2000,0342	Schamberger																		X									X					
MUH-12656	Hartmann																		X									X					
MUH-12666	Walter																		X									X					
P2000,0361	Dickenscheid																		X									X					
P2000,0341	Kaiser																		X									X					
P2000,0344	kaiser																		X									X					
GR97P1861D	Weinrich	X																									7						Faxed
A-2834	Knabe	10																															
GR97P1903	Reichert	9																															
A-2845	Richter	10																					1						$110.00		X		
GR00P23423	Grassmann	9																						X									
MAS-FIN-203	Barchmann																										1						
A-2972	Sommer																						2	X			3		$410.00		X		Decl. 37 CFR, Invention Discl.
L&L-I0078	Kersch																						1			X			$860.00		X		
MAS-FIN-235	Goller	13																															
A-8215	Lorenzi	9								X															X								

Lerner and Greenberg, P.A.

Mail Docket
2003

DOCKET NO.	INVENTOR	Amend (No. of Pgs.)	Amend 1.116 (No. of Pgs.)	Appeal	Application (No. of Pgs.)	Assignment	Brief	Cert. Correction	CIP	Claim for Priority	Declaration	Divisonal	Express	Fil. Rcpt. Correct.	Formal Drawings (No.)	IDS (No. of Refs.)	Inf. Drawings (No.)	Issue Fees	Letter	Letter Draftsman	Maintenance Fee	PCT Cover Sheet	Petition for Ext.	(Ass.) Power of Attorney	Priority Document	RCE	Response	Trademark Application	1533	$ Amount	$ Amount	Credit Card	Check	Addit. Info.
23-Oct-03																																	
J&R-0854	Reithofer	19																															
P2001,0294	Kupnik									X	X								X						X					$130.00		X		
W&B-INF1951	Beer									X	X								X						X					$130.00		X		
W&B-INF1964	Kaiser									X	X								X						X					$130.00		X		
S&Z-IO030901	Däche										X								X											$130.00		X		
MAS-FIN-409	Hagen									X	X								X						X					$130.00		X		
W&B-INF1957	Beer									X	X								X						X					$130.00		X		
L&L-I0223	Krüger									X														X	X								
F-8164	Vanmoor										X								X														
GR99P1679	Deboy																																
MUH-12619	Ruckerbauer													X																			
ZTP98P4050D	Kaiser													X																			
M&N-IT-101	Mueller		10																														
GR00P1339	Stolze	12																															
GR00P4091	Beitel		9																														
IN-1073D	Schrems	17																															cert. Translation
S&Z-IO020307	Kakoschke															7								X									
P2001,0216	Cappellani															2								X									Taiwanese Office action
J&R-0854	Reithofer															2								X									European Search Report
A-3444	Becker														1					X				X									
J&R-0926	Verbeck					X												X											$1,630.00	$40.00	X		Publication Fee
ZTG99P16409	Strolz		1			X												X											$1,630.00	$40.00	X		Publication Fee
ZTG99P16409	Strolz															2																	
GR99P2859	Kopetzky																						1			X			$880.00		X		

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: P2001,0216 Appl. No.: Applicant: ANNALISA CAPPELLANI ET AL. Filing Date: September 26, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	6,091,120	7/18/00	Yeom et al.			
	B	5,089,863	2/18/92	Satoh et al.			
	C	5,384,479	1/24/95	Taniguchi			
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	42 34 528 C2	4/15/93	Germany				
	K	42 34 777 A1	4/21/94	Germany				
	L	2 791 177 A1	9/22/00	France				
	M	63044768	2/25/88	Japan				
	N	0 740 334 A2	10/30/96	Europe				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2nd Edition, pp. 201-203
		Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418

EXAMINER	DATE CONSIDERED

FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.: P2001,0216
Appl. No.:

Applicant: ANNALISA CAPPELLANI ET AL.

Filing Date: September 26, 2003
Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
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FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	0 328 350 A2	8/16/89	Europe				
	K	02/41383 A1	5/23/02	WIPO				
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of $TiSi_2$ and $CoSi_2$ ", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269
		Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1-μm CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956

EXAMINER	DATE CONSIDERED

FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.: P2001,0216
Appl. No.:

Applicant: ANNALISA CAPPELLANI ET AL.

Filing Date: September 26, 2003
Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
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	G						
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	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs", IEEE, 1994, pp. 497-500

EXAMINER

DATE CONSIDERED

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 63044768
PUBLICATION DATE : 25-02-88

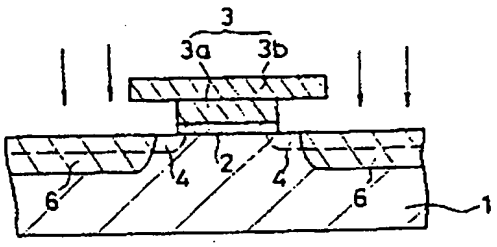
APPLICATION DATE : 12-08-86
APPLICATION NUMBER : 61188815

APPLICANT : MITSUBISHI ELECTRIC CORP;

INVENTOR : SATO SHINICHI;

INT.CL. : H01L 29/78

TITLE : FIELD EFFECT TRANSISTOR AND MANUFACTURE OF THE SAME



ABSTRACT : PURPOSE: To neutralize a negative potential by a positive voltage applied to a gate electrode even if hot electrons are trapped by an insulating film by a method wherein a gate electrode of a T-shape cross-section is formed on a required part of a substrate and the insulating film is buried between the part of the gate electrode close to the substrate surface and the substrate surface beneath the electrode.

CONSTITUTION: After a gate insulating film 2 is formed on a silicon substrate 1, the material for a gate electrode 3 is applied. The gate electrode material is a double-layer film composed of, for instance, a polycrystalline silicon layer 3a and a high melting point metal layer 3b. By applying plasma etching to the electrode materials 3a and 3b with optimized conditions such as gas composition, gas pressure and electric power, a gate electrode 3 of a T-shape cross-section which has a brim part is formed. Then low concentration diffused layers 4 are provided closer to the gate electrode than high concentration diffused layers 6 and those two type diffused layers form continuous double-layer structures. With this constitution, a highly reliable transistor in which creation of hot carriers is suppressed and the gm deterioration caused by the carriers trapped by the insulating film is avoided can be obtained.